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REMARKS

Claims 1-27, all the claims pending in the application, stand rejected on prior art grounds. Claims 4, 6, 11, 13, 18, 20, 24, and 26 stand rejected upon informalities. In addition, the drawings and specification are objected to. Claims 1-2, 8-9, 15-16, and 21-22 are amended herein. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The Objections to the Specification

The specification stands objected to because of informalities. As such, Applicants have amended the specification to overcome the objections noted in the Office Action. Specifically, Applicants have amended paragraphs [0020], [0025], [0030], and [0034] in order to more clearly and accurately describe the claimed invention. Thus, the Applicant respectfully requests that these objections be reconsidered and withdrawn.

II. The Objections to the Drawings

The drawings stand objected to as well. Applicants have amended Figures 2 and 3 to overcome the objections, with the changes shown in red. Moreover, Applicants herein submit new formal drawings (of all the figures) to overcome the objections noted in the Office Action as well as the "notice of Draftsperson's Patent Drawing Review." Specifically, elements 11, 13, 15, and 102 in Figure 3 are labeled according to their respective functions. Reference to element 6 is removed from the specification as provided herein (see amended paragraph [0034] above).

Figure 2 is amended to include the comparator 800, which was mistakenly omitted in the original drawings submitted with the application. However, page 6, paragraph [0028] of the specification clearly indicates that Figure 2 comprises a comparator 800. As such, no new matter is being added.

With regard to the resistors as described in claims 2, 9, 16, and 22, the Office Action indicates that these elements are not shown in the drawings. However, on page 8, paragraph [0032] of the specification, it states that, "The ideal resistance values are estimated by tracing the netlist from a supply to the least resistive path and adding the resistors along the path." This, along with the claimed language, indicates that the resistors constitute part of the net 605 illustrated in Figure 2, and as such have not been individually drawn in the figures to prevent unnecessary ambiguity of the claimed invention. However, those skilled in the art would readily understand, upon reading the specification and claims in conjunction with the drawings that the resistors are provided in the net(s) 605. Thus, the Applicant respectfully requests that these objections be reconsidered and withdrawn.

III. The Objections to the Claims

Claims 2, 9, 16, and 22 are objected to because the Office Action indicates that "a supply" is incomplete. As such, Applicants have amended these claims to indicate that the supply is a "power supply", which is properly supported in various paragraphs of the specification as originally filed. Thus, the Applicant respectfully requests that these objections be reconsidered and withdrawn.

IV. The 35 U. S.C. §112, Second Paragraph, Rejections

Claims 4, 6, 11, 13, 18, 20, 24, and 26 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. Specifically, these claims are rejected because the Office Action suggests that the phrase "area and perimeter values" are not clearly defined in the specification, drawings, and claims. Applicants respectfully traverse these rejections as explained below.

According to the invention, the nets interconnect the ports on various logic cells and serve as the wiring connection for the circuit (see pages 1-2, paragraph [0006] of the specification as originally filed). Moreover, pages 9-10, paragraph [0037] of the specification as originally filed describes the geometric characteristics of the wire widths associated with the nets. As such, these wires not only have a width associated with them, but also a length, as further described in paragraph [0037]. The area and perimeter values are calculated from the wire widths and lengths, and these values are clearly dependent on the various combinations of these parameters, which are different depending on the specific embodiment used. Those skilled in the art would acknowledge and understand that the area and perimeter values are not static from embodiment to embodiment, and as such only a general framework of understanding how the invention utilizes these values is necessary for those skilled in the art to practice the invention. As such, paragraphs [0014], [0027], and [0038] clearly describe how the invention utilizes the area and perimeter values in estimating the maximum parasitic impedance. Therefore, the

Examiner is respectfully requested to reconsider and withdraw these rejections.

V. The Prior Art Rejections

Claims 1-27 stand rejected under 35 U.S.C. §102(b) as being anticipated by Ho (U.S. Patent No. 5,903,469). Claims 1-3, 8-10, 15-17, and 21-23 rejected under 35 U.S.C. §102(b) as being anticipated by Murai (U.S. Patent No. 6,138,267). Applicants respectfully traverse these rejections based on the following discussion.

A. The Ho Reference

Ho teaches a method of extracting layout parasitics for nets of an integrated circuit. The method creates a connectivity-based database (1104), where geometries of a layout are organized by nets of the circuit schematic. The method permits net-by-net extraction (1124) of layout parasitics using a connectivity-based database. A user can select a net or nets for extraction. A net is decomposed into polygon subsections, and parasitics are determined for these subsections. Layout parasitics for some of the decomposed geometries may be found in a predefined geometry library. A database is created containing nets and their extracted layout parasitics (1132). A netlist format file may be generated from this database of extracted parasitics to provide for back annotation of layout parasitics into a circuit schematic for further circuit analysis.

B. The Murai Reference

Murai teaches a semiconductor integrated circuit reliability verification device for

detecting any portion of design that may cause circuit malfunction due to the effects of switching noise, comprises a partial circuit network detecting part for detecting, based on a transistor-level net list for the circuit to be verified, information concerning partial circuit networks that form part of a circuit to be verified, a maximum resistance calculating part for calculating, based on the information concerning the partial circuit network, the maximum resistance that occurs while the channel connected component is operating, a gate capacitance calculating part for calculating, based on the information concerning the partial circuit network, the total gate capacitance for the portions but the inverter of a driven circuit, and an error judging part for calculating the value of evaluation function, based on the value of maximum resistance and the total gate capacitance, and judging whether or not the calculated value is in violation of the design criteria.

C. Applicants' Response

As amended independent claims 1, 8, 15, and 21 contain features, which are patentably distinguishable from the prior art references of record. Specifically, the claims 1, 8, and 21 recite, in part, "[a] method for performing parasitic extraction for a component having a plurality of nets and ports, said method comprising...categorizing said nets for their parasitic accuracy needs based on a comparison of said minimum output impedance with said maximum parasitic impedance." Similarly, claim 15 recites, in part, "...wherein said nets are categorized for their parasitic accuracy needs based on a comparison of said minimum output impedance with said maximum parasitic impedance."

These features are simply not taught or suggested in the prior art references of record,

namely Ho or Murai. For example, the Office Action suggests that Ho teaches calculating a minimum output impedance (figs. 9-18) for each port (figs. 1-5, 8, 25-27). However, none of the cited Figures 9-18, nor any of the descriptions of these respective figures, nor any of the other descriptions elsewhere in Ho discuss impedance, or a minimum output impedance, let alone calculating the minimum output impedance. While Ho discusses resistance and capacitance, it does not adequately describe inductance calculation, which the claimed invention clearly provides in its recitation of the word "impedance". Furthermore, Ho does not describe categorizing the nets based their parasitic accuracy needs. Additionally, Ho teaches a layout database for back annotation for extraction values. However, Ho does not discuss calculating lower and upper bounds (minimum and maximum impedances) as does the claimed invention. Moreover, the claimed invention first determines these lower and upper bounds (minimum and maximum impedances), creates impedance error requirements for all ports, and then uses this information to simplify and reduce the extraction effort in a far more efficient and beneficial manner than Ho. Thus, the claimed invention use the lower/upper bounds to guide the extracted values, which Ho does not do.

Likewise, the Office Action suggests that Murai teaches calculating a minimum output impedance (figs. 1-2, 10) for each port (figs. 3-9). However, none of the cited Figures 1-2 and 10, nor any of the descriptions of these respective figures, nor any of the other descriptions elsewhere in Murai discuss impedance, or a minimum output impedance, let alone calculating the minimum output impedance. While Murai discusses resistance and capacitance, it does not adequately describe inductance calculation, which the claimed invention clearly provides in its

recitation of the word "impedance". Furthermore, Murai does not describe categorizing the nets based their parasitic accuracy needs. Additionally, Murai teaches coupled noise extraction, which is different from the claimed invention.

The claimed invention greatly simplifies the parasitic impedance extraction process by reducing the timing (run times) and increasing the efficiency in which parasitic extraction process occurs. This feature is a significant step forward from the processes and systems described in either Ho or Murai. Moreover, the claimed invention has the ability to determine what the accuracy requirements are for every net. Additionally, the claimed invention provides for a more accurate and more complex parasitic resistance and capacitance model and a more accurate detailed parasitic extraction process without increasing run times by comparing the maximum estimates with the minimum port impedances, which allows the ability to categorize the nets for their parasitic accuracy needs, which are features not taught or suggested in either Ho or Murai.

Furthermore, the claimed invention simplifies the decision process in TD (Trapezoidal Decomposition) by determining, at the beginning of the decision tree, which shapes can be skipped thereby improving the capacitance extraction performance. Also, the claimed invention compares a quick estimate of the expected parasitic values with the already existing schematic values, which allows the circuit designer to set the accuracy level and to decide whether the parasitic value is needed at all. Again, these features are not taught or suggest in either Ho or Murai.

In view of the foregoing, the Applicants respectfully submit that the cited prior art do not

teach or suggest the features defined by amended independent claims 1, 8, 15, and 21 and as such, claims 1, 8, 15, and 21 are patentable over either Ho or Murai. Further, dependent claims 2-7, 9-14, 16-20, and 22-27 are similarly patentable over either Ho or Murai, not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the invention they define. Thus, the Applicant respectfully requests that these rejections be reconsidered and withdrawn.

Moreover, the Applicant notes that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

VI. Formal Matters and Conclusion

With respect to the objections to the specifications and claims, the specification and claims have been amended, above, to overcome these objections. With respect to the objection to the drawings, a Submission of Proposed Drawing Corrections is submitted herewith. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objections to the specification, claims and drawings and rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-27, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the

Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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